UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,472	02/19/2002	Maitreyee Mahajani	40025-005	6706

33971 7590 06/01/2004

MATRIX SEMICONDUCTOR, INC.
3230 SCOTT BOULEVARD
SANTA CLARA, CA 95034

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,472	MAHAJANI ET AL.	
	Examin r	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3,5-9,12-15,20-34 and 36-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3,5-9,12-15,20-34 and 36-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 9, 12-15, 20-21, 24, 26, 27, 30-31; and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pub 2003/0017670 to Luoh et al.

Regarding to claims 9, 24 Louh discloses a method for making a SONOS device, comprising: providing a channel region (area between source and drain 19 [0019]), and providing a first oxide layer 13 on the channel region by ISSG process providing a nitride layer 14, on the first oxide layer 13, and providing a second oxide layer 16 on the nitride layer [0020], wherein the device is a SONOS.

Regarding to claims 12-15, 20 Louh discloses a method wherein the ISSG is performed at a temperature ranging from 600°C to about 900°C, wherein the pressure ranging from 100

millitorr to about 760 torr [0020], wherein the ISSG oxide layer 13 having the thickness of 10 to about 200 angstrom [0023], wherein the transistor is a SONOS transistor, 10= silicon, 13 = oxide, 14=nitride, 16 = oxide, 17 = silicon [0018], wherein the method further including annealing the oxide layer in a nitric oxide atmosphere [0022].

Regarding to claims 21, 26 Louh discloses a method for making a gate dielectric structure for a SONOS device comprising: providing silicon 10, providing an oxide layer 13 of gate dielectric structure on the silicon 10 by ISSG [0020], the oxide layer having a thickness of about 10 to 200 angstrom [0023] and annealing the oxide layer in a nitric oxide atmosphere [0022], wherein the device is a SONOS device.

Regarding to claims 27, 34, Louh discloses a method for making a transistor containing a gate dielectric structure, comprising: providing a gate conductor 17 [0018], providing a channel region (area between source and drain 19 [0019]), and providing between the gate conductor 17 and the channel, an oxide layer 13 of the gate dielectric structure by ISSG, wherein the transistor device is a SONOS transistor.

Regarding to claims 30, 31; Louh discloses the method wherein the silicon is a surface of silicon wafer, wherein the silicon comprises polysilicon. Although the prior art does not specially disclose the claimed silicon wafer, this feature is seen to be inherent teaching of that limitation because the semiconductor substrate 10 would be understood in the art as comprising silicon wafer or polysilicon.

3. Claims 9, 12-15, 21-22, 24, 26-27, 30-31, 34-40 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6674138 to Halliyal et al.

Regarding to claims 9, 24 Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, column 9 line 1, and providing a first oxide layer 28 on the channel region by ISSG process, column 10 line 33, providing a nitride layer 30, on the first oxide layer 28, and providing a second oxide layer 32, column 8 line 63, on the nitride layer 30, wherein the device is a SONOS.

With respect to nitride layer 30, Halliyal discloses structure 26 is an ONO structure, column 8 line 27; thus Halliyal either inherently or implicitly discloses nitride layer.

Regarding claims 12-15, Halliyal discloses a method wherein the ISSG is performed at a temperature ranging from 700°C to about 1150°C, column 11 line 17, wherein the pressure ranging from 100 torr to about 300 torr, column 11 line 9, wherein the ISSG oxide layer 28 having the thickness of 10 to about 150 angstrom, column 11 line 65, wherein the transistor is a SONOS transistor, wherein the method further including annealing the oxide layer 18 in a nitric oxide atmosphere, column 7 line 39.

Regarding claims 21, 22, 30, 31 Halliyal discloses a method for making a gate dielectric structure for a SONOS device comprising: providing silicon 16, providing an oxide layer 28 of a gate dielectric structure on the silicon by in-situ steam generation, column 10 line 33, the oxide layer having a thickness of about 10 to about 150 angstroms, column 11 line 65, and annealing the oxide layer in a nitric oxide atmosphere, column 7 line 39, wherein the device is a SONOS device, wherein silicon is silicon layer or polysilicon, column 10 lines 1-3. Regarding claim 22, Halliyal discloses a method for making a SONOS device, providing a gate conductor 24, column 5 line 6, providing a channel region 18, column 5 line 6, and providing between the gate

conductor and the channel region, an oxide layer 28 of a gate dielectric structure by an in-situ steam generation process, column 10 line 33, performed at a temperature ranging from about 700 to about 1150 degrees Celsius, column 11 line 17, a pressure ranging from about 100 torr to about 300 torr, column 11 line 9, and for a time sufficient to deposit an oxide thickness of about 10 to about 150 angstroms, column 11 line 65, wherein the device is a thin film transistor or a SONOS device.

Regarding claims 26-27, 34, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by the method comprising: providing silicon 16, column 10 line 3, providing a first oxide layer 28 on the silicon layer 16 by ISSG, column 10 line 33, providing a nitride layer on 30 on first oxide layer, and providing a second oxide layer 32, column 8 line 63, wherein the device is a SONOS device, wherein the gate 24 comprises metal, column 15 line 40.

With respect to nitride layer 30, Halliyal discloses structure 26 is an ONO structure, column 8 line 27; thus Halliyal either inherently or implicitly discloses nitride layer.

Regarding claims 36, 37 Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, providing a first oxide layer 28 in contact with the channel region by an in-situ steam generation process, column 10 line 33, providing a nitride layer 30 in contact with the first oxide layer; and providing a second oxide layer 32, column 8 line 63 in contact with the nitride layer, fig. 1.

With respect to nitride layer 30, Halliyal discloses structure 26 is an ONO structure, column 8 line 27; thus Halliyal either inherently or implicitly discloses nitride layer.

Regarding claim 38, Halliyal discloses an integrated circuit containing a SONOS semiconductor device made by a method comprising: providing a silicon wafer or silicon layer 16, fig. 1, providing a first oxide layer 28 in contact with the silicon wafer or silicon layer 16 by an in-situ steam generation process, column 10 line 33, providing a nitride layer 30 in contact with the first oxide layer; and providing a second oxide layer 32 in contact with the nitride layers, fig. 1, wherein the device is a SONOS semiconductor device.

With respect to nitride layer 30, Halliyal discloses structure 26 is an ONO structure, column 8 line 27; thus Halliyal either inherently or implicitly discloses nitride layer.

Regarding claim 39, Halliyal discloses a method for making a gate dielectric structure for SONOS device, comprising: providing a channel 18; providing an oxide layer 28 of a gate dielectric structure in contact with the channel by in-situ steam generation, column 10 line 33, the oxide layer having a thickness of about 10 to about 150 angstroms, column 11 line 65; and annealing the oxide layer in a nitric oxide atmosphere, column 7 line 39, wherein the device is a SONOS device.

Regarding claim 40, Halliyal discloses a method for making a gate dielectric structure for a thin film transistor or a SONOS device, comprising: providing a gate conductor24, fig. 1, providing a channel region 18; and providing, between the gate conductor 24 and the channel region 18 and in contact with the channel region 18, an oxide layer 28 of a gate dielectric structure by an in-situ steam generation process, column 10 line 33, performed at a temperature ranging from about 700 to about 1150 degrees Celsius, column 11 line 17, a pressure ranging from about 100 torr to about 300 torr, column 11 line 9, and for a time sufficient to deposit an

oxide thickness of about 10 to about 150 angstroms, column 11 line 65, wherein the gate dielectric structure is for a thin film transistor or a SONOS device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 3, 5-8, 22-23, 25, 28-29, 32-33 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5700699 to Han et al in view of US 6184155 to Yu et al

6. Regarding to claims 3, 23, 25, and 41-42, Han discloses a method for making a transistor containing a gate dielectric structure, comprising: providing a gate conductor 7, fig. 4, column 2 line 65, providing a channel (area between 4 and 5), and providing between the gate conductor 7 and the channel and in contact with the channel region an oxide laver 12 of the gate dielectric structure, wherein the transistor is a thin film transistor.

However, Han does not disclose an oxide layer 12 by an in-situ steam generation process (ISSG).

But Yu reference discloses the oxide layer 4b fig. 3 column 3 line 32 by ISSG. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to combine the oxide layer 4b by ISSG of Yu to replace the method of making layer 12 of Han, because it would have created a thin gate oxide layer with reduction in leakage current, during standby, or operating modes as taught by Yu, see abstract.

Regarding claims 5-8, Han does not discloses the method wherein the in-situ steam generation process is performed at a temperature ranging from about 600 to about 900 degree Celsius, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, further including annealing the oxide layer in a nitric oxide atmosphere.

However, Yu discloses the method wherein the in-situ steam generation process is performed at a temperature ranging from about 600 to about 900 degree Celsius, column 3 line 27, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, column 3 line 33, further including annealing the oxide layer in a nitric oxide atmosphere, column 3 line 28. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the method of making the oxide layer 4b of teaching of Yu to replace the method of making the oxide layer 12 of Han, because it

would have created a thin gate oxide layer with reduction in leakage current, during standby, or operating modes as taught by Yu, see abstract.

Regarding claims 22, 40 as discussed in the above claims 3, 5-7, the combination of Han, Yu discloses all the limitations of claim 22.

Regarding claims 28-29, 32-33, Han discloses a method wherein the transistor is a SONOS transistor (polysilicon 3, oxide 12, nitride13, oxide 14, polysilicon 7), wherein the transistor comprises a floating gate 7.

7. Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5700699 to Han et al in view of US Pub 2003/0017670 to Louh et al.

Regarding to claims 3, 5-8, 23, 25 Han discloses a method for making a transistor containing a gate dielectric structure, comprising: providing a gate conductor 7, fig. 4, column 2 line 65, providing a channel (area between 4 and 5), and providing between the gate conductor 7 and the channel an oxide laver 12 or 15 of the gate dielectric structure, wherein the transistor is a thin film transistor.

However, Han does not disclose an oxide layer 12 by an in-situ steam generation process (ISSG), wherein the in-situ steam generation process is performed at a temperature ranging from about 600 to about 900 degree Celsius, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, further including annealing the oxide layer in a nitric oxide atmosphere.

But Louh reference discloses the oxide layer 13, fig. 2, is formed, by ISSG [0020], wherein ISSG is performed at a temperature ranging from about 800 to about 1200 degree Celsius, wherein the in-situ steam generation process is performed at a pressure ranging from about 10 torr to about 760 torr [0020], wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 5 to about 30 angstroms [0023], further including annealing the oxide layer in a nitric oxide atmosphere [0020]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG oxide layer 13 by ISSG process teaching of Louh to replace the method of making layer 28 Halliyal, because it would have created a high reliability dielectric layer for memory device as taught by Louh [0002].

Regarding claims 28-29, 32-33, Han discloses transistor is a SONOS comprising a floating gate 7.

Regarding claims 41-42, Han discloses a thin film transistor containing a gate dielectric structure made by a method comprising: providing a gate conductor 7, fig. 4, providing a channel region 3, and providing between the gate conductor and the channel region and in contact with the channel region, an oxide layer 12 of the gate dielectric structure on the channel region, wherein the transistor is a thin film transistor.

However, Han does not disclose an oxide layer 12 by an in-situ steam generation process (ISSG).

But Louh reference discloses the oxide layer 13, fig. 2, is formed, by ISSG [0020]. At the time the invention was made; it would have been obvious to one of

ordinary skill in the art to use the ISSG oxide layer 13 by ISSG process teaching of Louh to replace the method of making layer 28 Halliyal, because it would have created a high reliability dielectric layer for memory device as taught by Louh [0002].

8. Claims 3, 5-8, 23, 25, 28-29, 32-33, and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US PUB 2003/0017670 to Louh et al. in view of US 5700699 to Han et al.

Regarding claims 3, 5-8, 23, 28-29, 32-33, and 41-42, as discussed in the above claims 9, 12-15, Louh discloses all limitations of claims 3, 5-8, 23, 28-29, 32-33, and 41-42, except Louh does not expressly disclose the device is a thin film transistor. It would have been obvious to one of ordinary skill in the art to use the ISSG teaching of Louh to form a device for intended use such as thin film transistor for the LCD device, because such device is conventional in the art as it being disclosed by Han, fig. 4, column 1 line 6-7 and would have a high-reliability dielectric layer as taught by Louh [0002].

9. Claims 9, 12-15, 21, 24, 26-27, 30-31, 34, 36-40 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6319775 to Halliyal et al. in view of US Pub 2003/0017670 to Louh et al.

Regarding to claims 9, 12-15, Halliyal discloses a method for making a SONOS device, comprising: providing a channel region 18, fig. 1, and providing a first oxide layer 28, column 4 line 61, on the channel region 18, fig. 1, providing a nitride layer 30, column 4 line 44, on the first oxide layer 28, and providing a second oxide layer 32, column 5 line 41, on the nitride layer 30, wherein the device is a SONOS.

However, Halliyal does not disclose an oxide layer 38 is formed by an in-situ steam generation process (ISSG), wherein the in-situ steam generation process is performed at a temperature ranging from about 600 to about 900 degree Celsius, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms, further including annealing the oxide layer in a nitric oxide atmosphere.

But Louh reference discloses the oxide layer 13, fig. 2, is formed, by ISSG [0020], wherein ISSG is performed at a temperature ranging from about 800 to about 1200 degree Celsius, wherein the in-situ steam generation process is performed at a pressure ranging from about 10 torr to about 760 torr [0020], wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 5 to about 30 angstroms [0023], further including annealing the oxide layer in a nitric oxide atmosphere [0020]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG oxide layer 13 by ISSG process teaching of Louh to replace the method of making layer 28 Halliyal, because it would have created a high reliability dielectric layer for memory device as taught by Louh [0002].

Regarding claims 21, 24 26-27, 34, 30, 31, 36-40, as discussed in the above claims 9, 12-15, the combination of Halliyal and Louh discloses all the limitation of claims 21, 24 26-27, 34, 30, 31, 36-40 including first gate oxide 28 is contact with the channel 16, the nitride layer 30 is

in contact with the first oxide layer 28, and the second oxide layer 32 is in contact with the nitride layer 30, see Halliyal fig. 1.

Response to Arguments

10. Applicant's arguments with respect to claims 3, 5-7, 22-23, 25, 28-29, 32-33, 36-42 have been considered but are moot in view of the new ground(s) of rejection.

11. With respect to Luoh reference, the Applicant argues that Luoh oxide layer 13 is not on the channel region, but instead on the conductive layer 12. Similarly, oxide layer 16 is not on nitride layer, but is instead on oxynitride layer 15. This is not persuasive because according to the Merriam Webster's Collegiate Dictionary defining the word 'ON' used as a function word to indicate the position in close proximity with and it does not necessarily mean 'in contact with'; therefore, Luoh reference would read on the claims 9, 12-15, 21, 24, 26, 27, and 30-31.

In response the Applicant's argument that the reference fails to show certain feature of Applicant's invention, it is noted that the feature upon which the Applicant relies, i.e. SONOS layers are being contiguous layers are not recited in the rejected claim. Although the claim are interpreted in light of the specification, limitation from the specification are not read into the claim, see In re Van Geuns, 988 F.22d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, it is proper to use the specification to interpret what the applicant meant by a word or phase recited in the claim. However, it is not proper to read the limitations appearing in the specification into the claim when these limitations are not recited in the claim; *Intervet America Inc. v. Kee-Vet Lab. Inc*, 887 F.2d 1050, 1053, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989). Furthermore, it is the claims that define the claimed invention, and it is claims, not specification that are anticipated or

unpatentable. Constant v. Advanced Micro Device Inc., 7 USPQ2d 1064. Therefore, Applicant cannot read limitations only set forth in the description into the claims for the purpose of avoiding the prior art. In re. Sporck, 386 F. 2d 924,155 USPQ 687 (CCPA 1967).

12. The Applicant argues that Han device is not a SONOS. The Examiner respectfully disagrees because a) Han discloses polysilicon 3= S, oxide 12 = O, nitride 13 = N, oxide 14 = O, and polysilicon 7 = S. Claims must be given their broadest interpretation, MPEP 2111; thus Han would read on the claim language, b) claim 3 recited 'wherein the transistor is a thin film transistor' and in claim 28 recited ' the method of claim 3, wherein the transistor is a SONOS transistor'; therefore, the statement 'the device is a SONOS device or is a thin film transistor' is a preamble generally is not accorded patentable weight where it merely recites the intended use of a structure, see MPEP 2111.02.

13. With respect to the multiple ISSG process disclosed by Yu, the claim language does not exclude such multiple ISSG process; thus Yu's reference would read on the claim language. In addition, claims must be given their broadest interpretation, see MPEP 2111.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le

LONG PHAM
PRIMARY EXAMINER